

野火_EBF6ULL S1 邮票孔核心板

目录

Page 1	目录
Page 2	历史版本
Page 3	CPU电源
Page 4	CPU PERI x1
Page 5	CPU PERI x2
Page 6	DDR3L
Page 7	eMMC/NAND FLAH
Page 8	BOOT CFG
Page 9	引出IO
Page 10	FUSE MAP
Page 11	
Page 12	

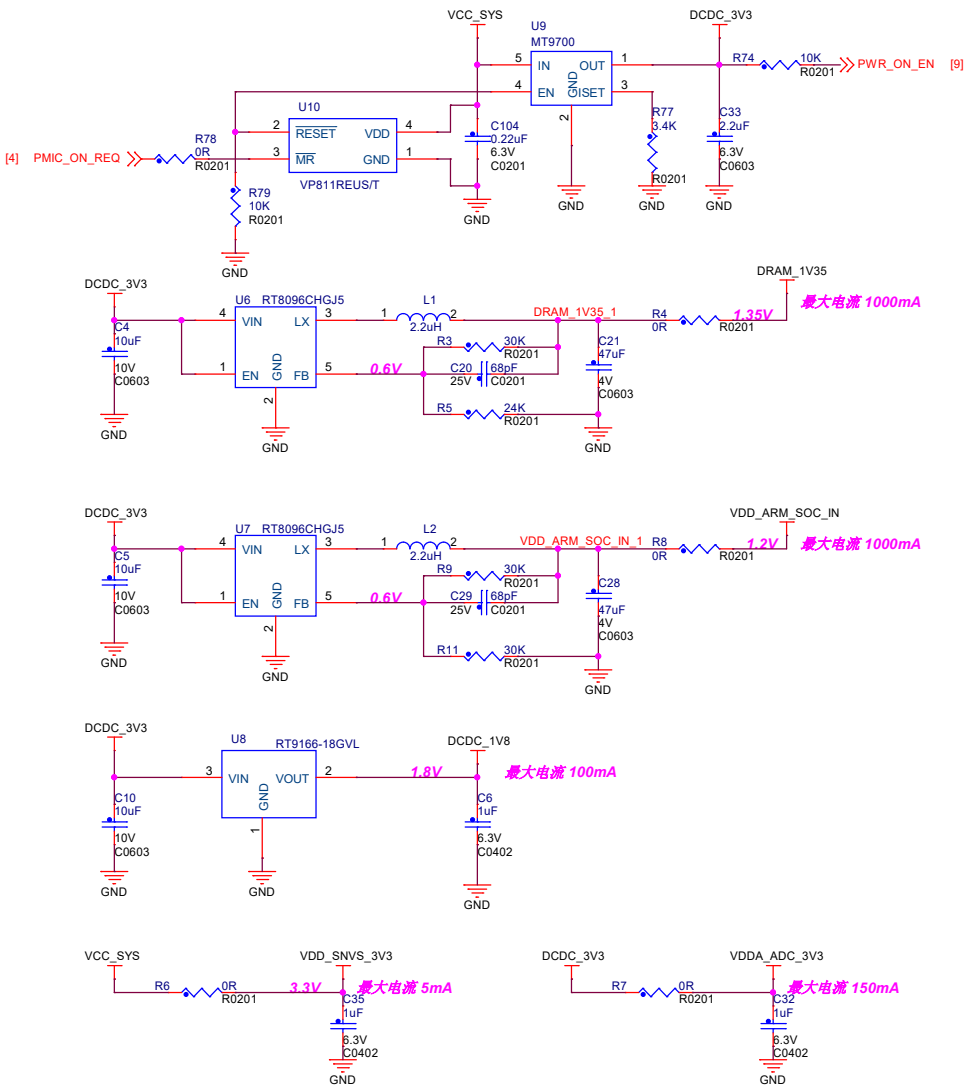
东莞野火电子有限公司 https://fire-stm32.taobao.com		
Title 野火_EBF6ULL S1 邮票孔核心板		
Size A3	Document Number 目录	Rev V1.0
Date: Saturday, December 10, 2022	Sheet 1	of 10

历史版本

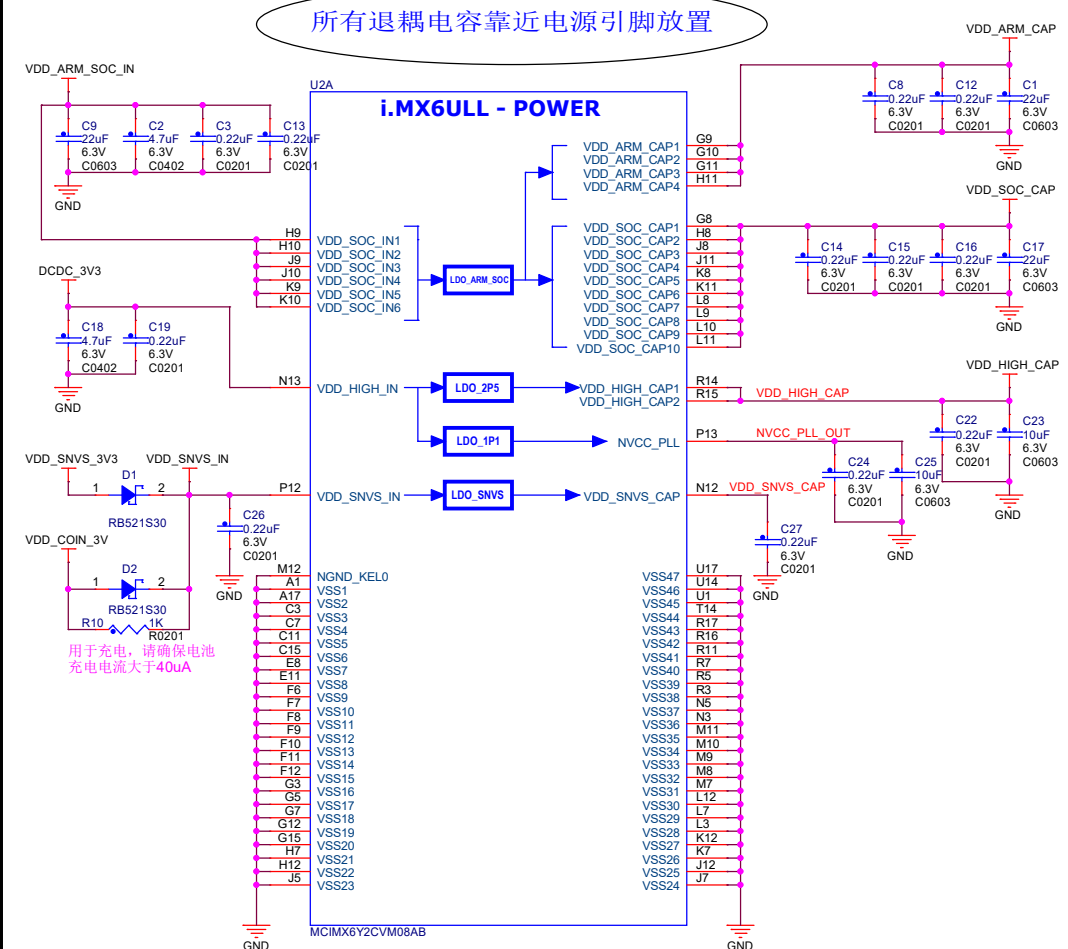
版本号	日期	设计	描述
V1.0	2019-05-30	cancore	初始版本, 开发阶段
V1.0	2019-08-15	cancore	整理对外发布, 稳定版

东莞野火电子有限公司 https://fire-stm32.taobao.com		
Title 野火_EBF6ULL S1 邮票孔核心板		
Size A3	Document Number 历史版本	Rev V1.0
Date: Saturday, December 10, 2022	Sheet 2	of 10

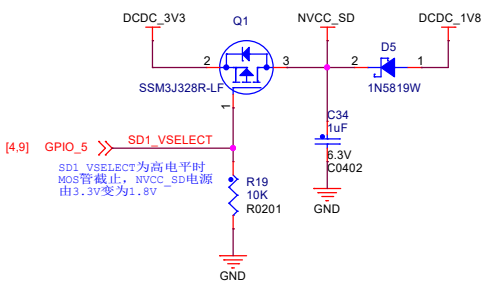
电源供电



MPU电源



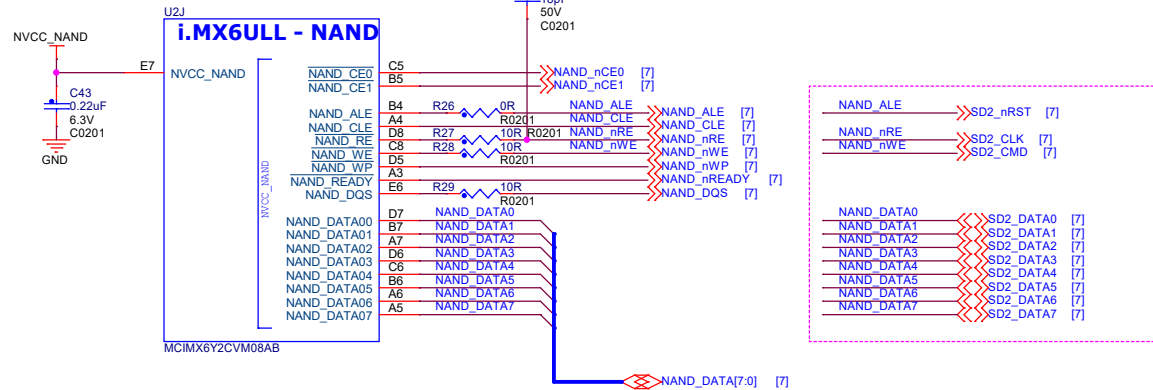
SD3.0供电切换电路



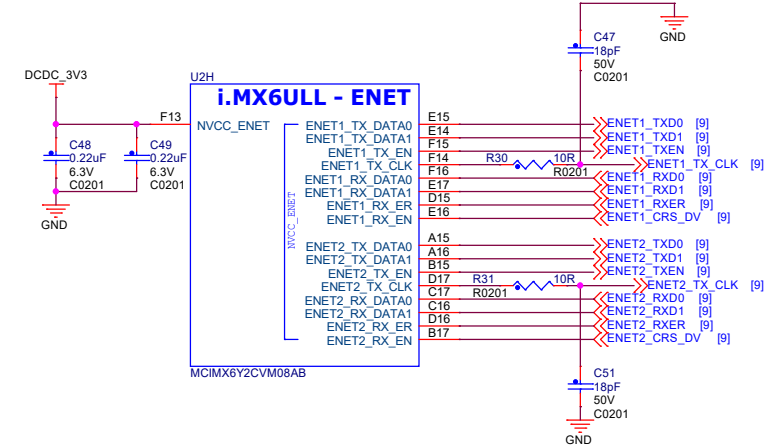
东莞野火电子技术有限公司 https://fire-stm32.taobao.com			
Title 野火_EBF6ULL S1 邮票孔核心板			
Size A3	Document Number CPU电源	Rev V1.0	
Date: Saturday, December 10, 2022	Sheet 3 of 10		

NAND/eMMC

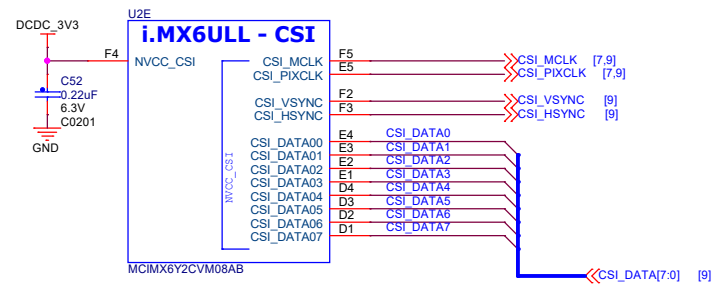
可以接nand flash也可以接eMMC



100M MII/RMII以太网

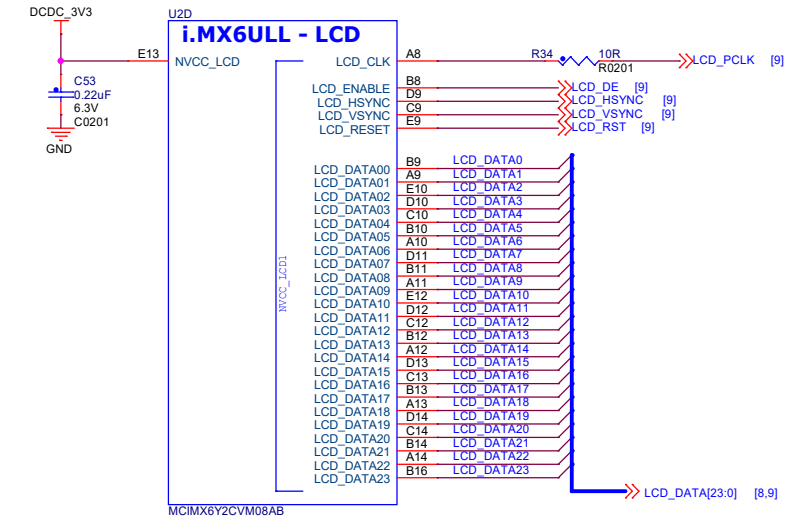


摄像头-8bit



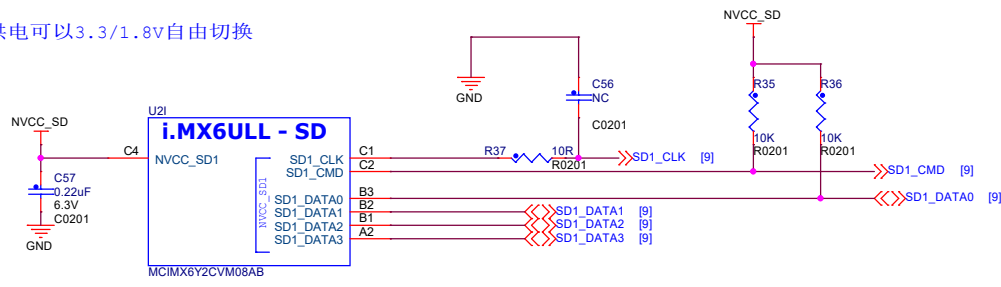
LCD888-24bit

最高支持分辨率为1366*768
最高支持像素时钟为85MHz

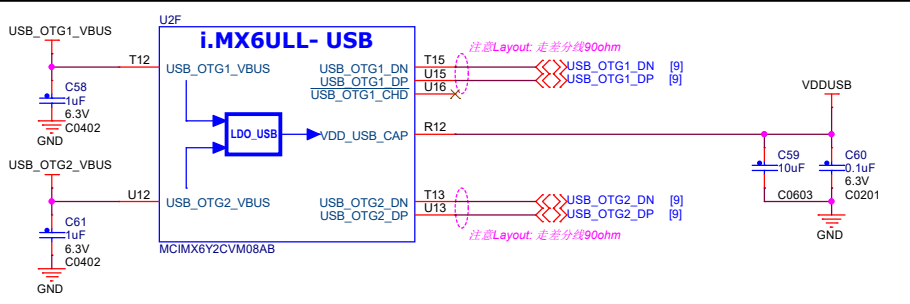


SD3.0

NVCC_SD供电可以3.3/1.8V自由切换

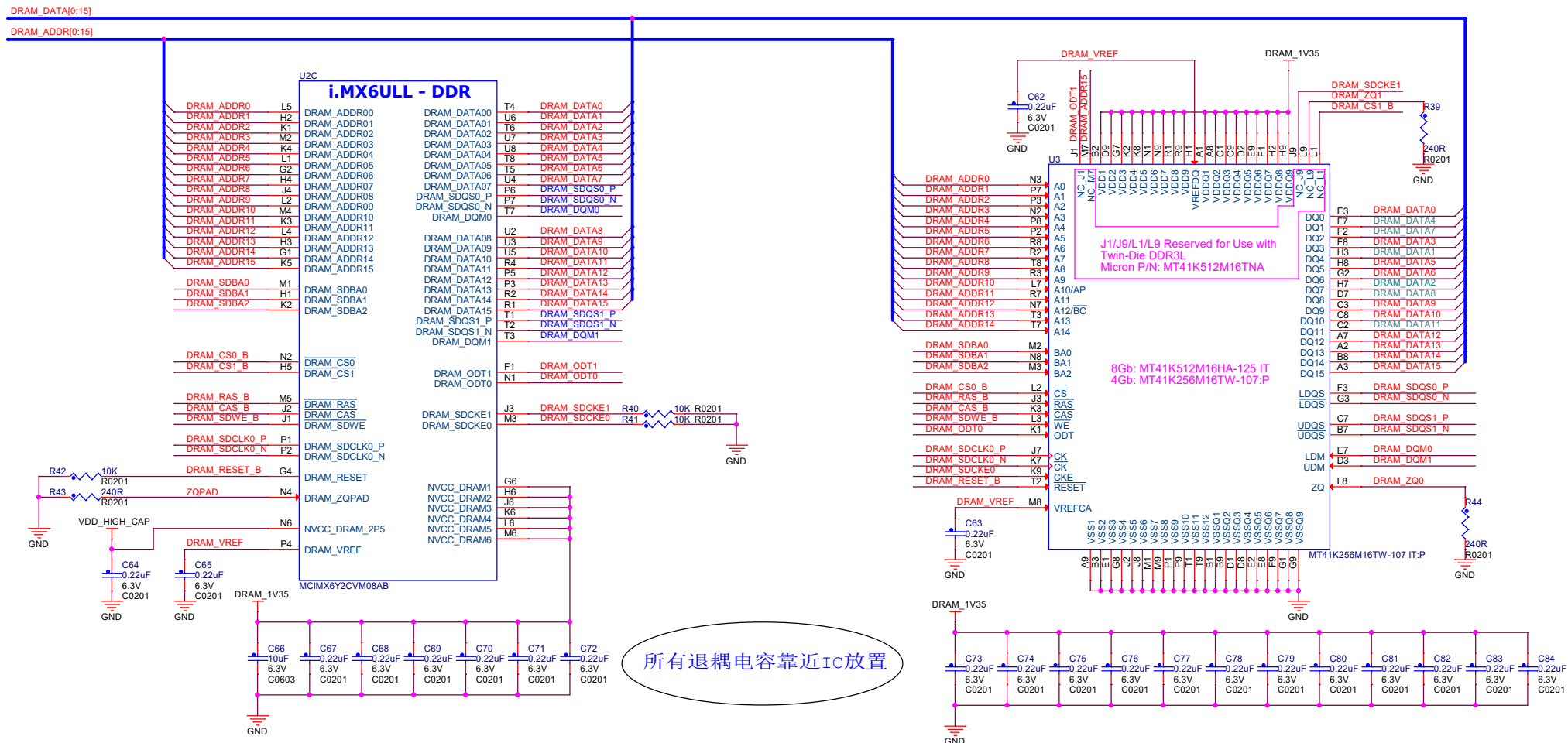


USB



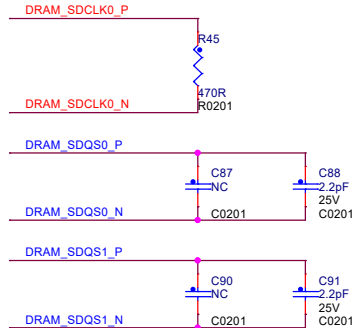
东莞野火电子技术有限公司 https://re-stm32.taobao.com		
Title 野火_EBF6ULL S1 邮票孔核心板		
Size A3	Document Number CPU PERI x2	Rev V1.0
Date: Saturday, December 10, 2022	Sheet 5 of 10	

DDR3L
默认容量为512M字节, 16位宽, 低电压1.35V

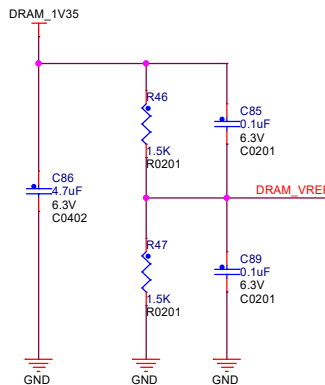


所有退耦电容靠近IC放置

CLK终端电阻: R45靠近DDR3放置

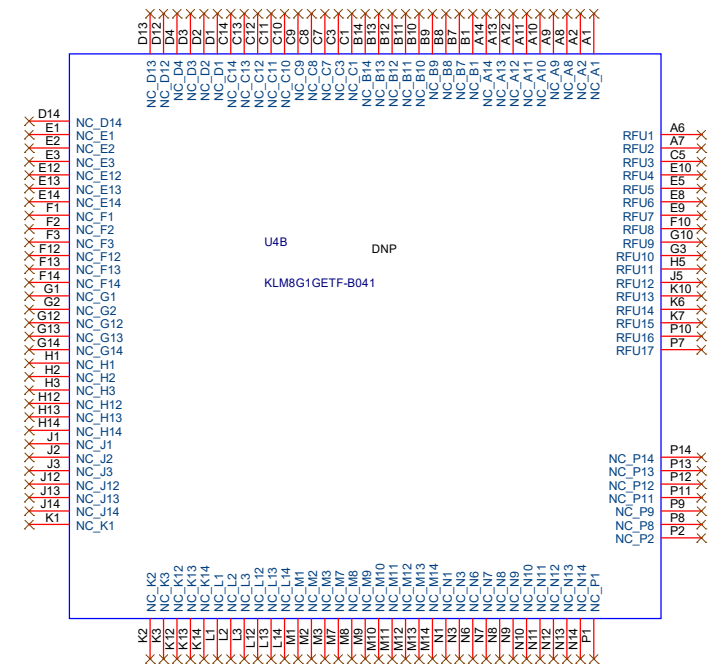
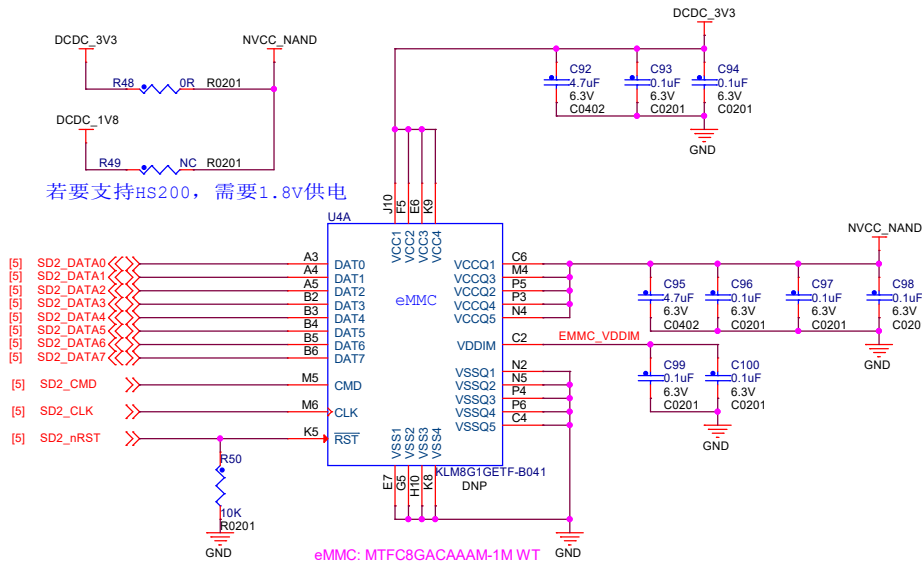


DDR3参考电压



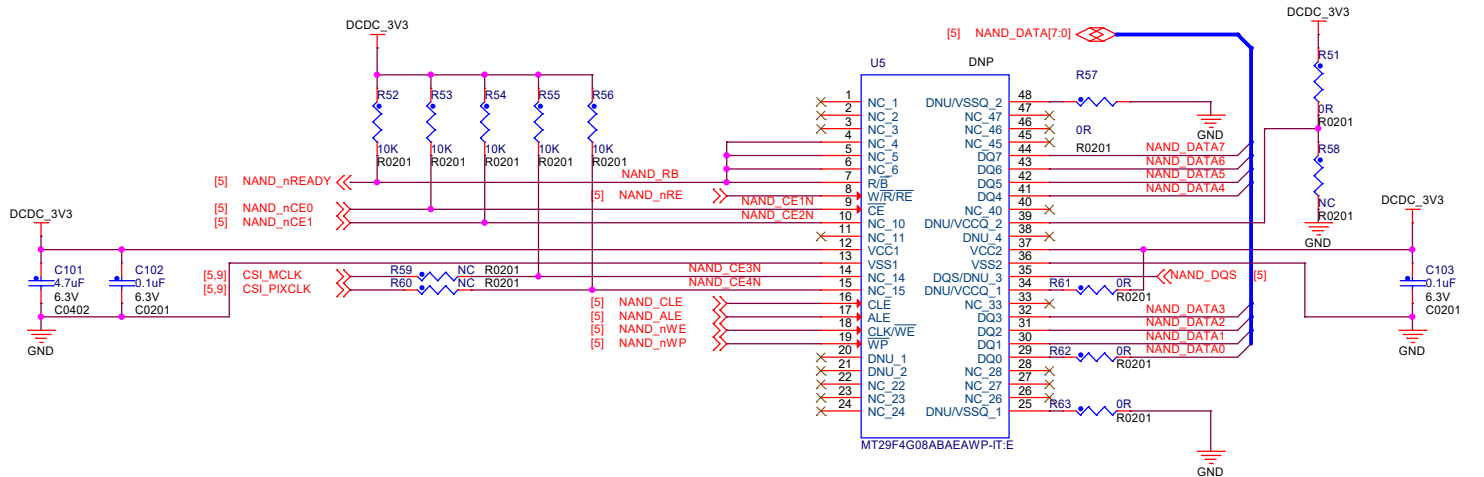
东莞野火电子技术有限公司 https://fire-stm32.taobao.com		
Title 野火_EBF6ULL S1 邮票孔核心板		
Size A3	Document Number DDR3L	Rev V1.0
Date: Saturday, December 10, 2022	Sheet 6 of 10	

eMMC
默认容量为8G字节

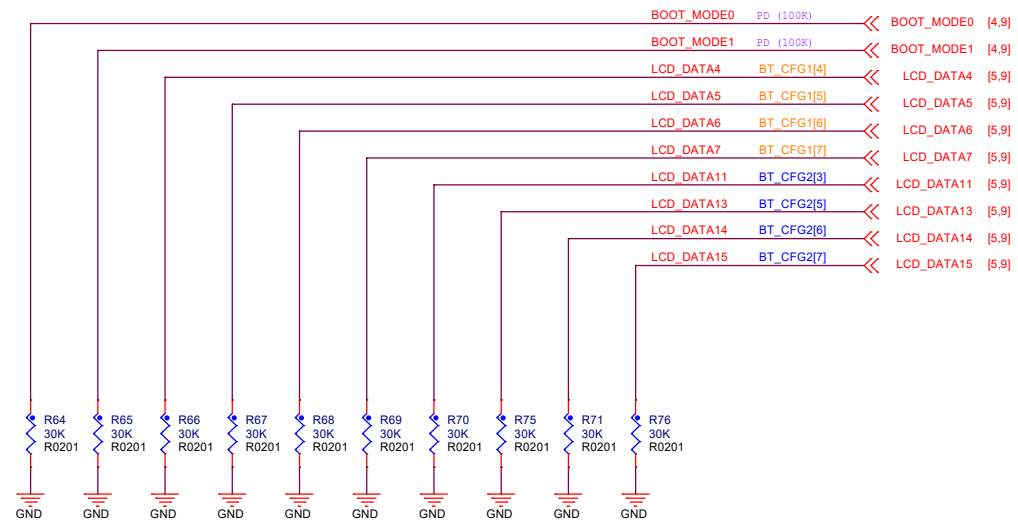


NAND FLASH

默认容量为512M字节, 8bit



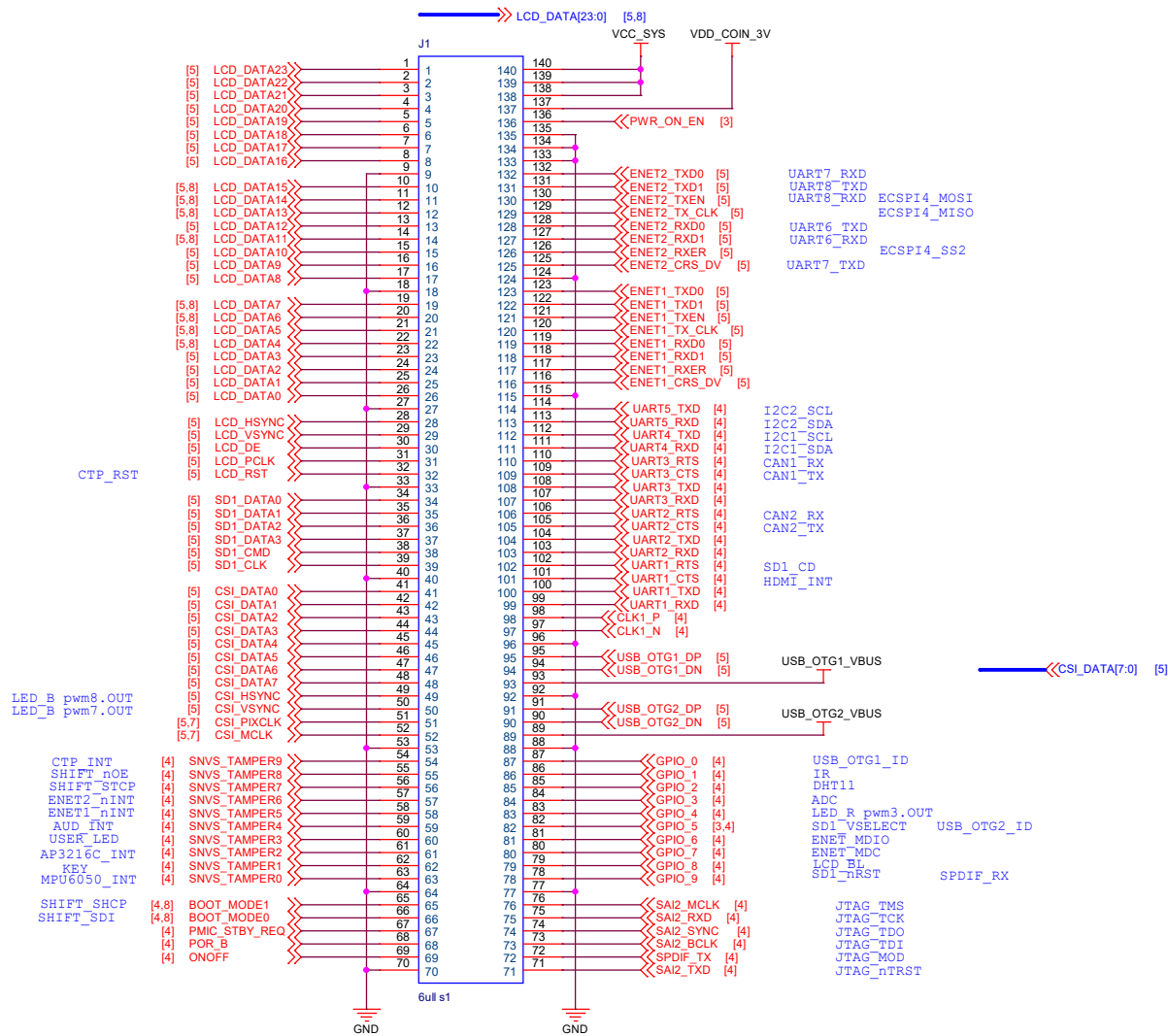
东莞野火电子技术有限公司 https://fire-stm32.taobao.com			
Title 野火_EBF6ULL S1 邮票孔核心板			
Size A3	Document Number eMMC/NAND FLASH	Rev V1.0	
Date: Saturday, December 10, 2022	Sheet 7 of 10		



东莞野火电子有限公司 https://fire-stm32.taobao.com		
Title 野火_EBF6ULL S1 邮票孔核心板		
Size A3	Document Number BOOT CFG	Rev V1.0
Date: Saturday, December 10, 2022	Sheet 8 of 10	

连接器

所有IO全部引出, 包括GPIO引出107个, 差分时钟一组, USB专用口2个, POR_B复位脚1个, 电源控制口2个



东莞野火电子技术有限公司 https://fire-stm32.taobao.com			
Title 野火_EBF6ULL S1 邮票孔核心板			
Size A3	Document Number 引出IO	Rev V1.0	
Date: Saturday, December 10, 2022	Sheet 9	of 10	

FUSE MAP

TYPE	BOOT_CFG1[7]	BOOT_CFG1[6]	BOOT_CFG1[5]	BOOT_CFG1[4]	BOOT_CFG1[3]	BOOT_CFG1[2]	BOOT_CFG1[1]	BOOT_CFG1[0]
QSPI	0	0	0	1	Reserved		DDR5MP: "000": Default "001-111"	
WEIM	0	0	0	0	Memory Type: 0 - NOR Flash 1 - OneNAND	Reserved	Reserved	Reserved
Serial-ROM	0	0	1	1	Reserved	Reserved	Reserved	Reserved
SD/eSD	0	1	0	Fast Boot: 0 - Regular 1 - Fast Boot	SD/eMMC Speed 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104	SD Power Cycle Enable 0 - No power cycle 1 - Enabled via USDMC_CS3 pin (USDMC3 & 4 only)	SD Loopback Clock Source 0 - SDR50 and SDR104 only 1 - Direct	
MMC/eMMC	0	1	1	Fast Boot: 0 - Regular 1 - Fast Boot	SD/MMC Speed 0 - High 1 - Normal	Fast Boot Acknowledge (Disable) 0 - Boot Ask Enabled 1 - Boot Ask Disabled	SD Power Cycle Enable 0 - No power cycle 1 - Enabled via USDMC_CS3 pin (USDMC3 & 4 only)	SD Loopback Clock Source 0 - SDR50 and SDR104 only 1 - Direct
NAND	1	BT_TOGGLEMODE	Pages in Block: 00 - 32B 01 - 64 10 - 32 11 - 256		Nand Number Of Devices: 00 - 1 01 - 2 10 - 4 11 - Reserved		Nand_Rom_address_Bytes: 00 - 2 01 - 4 10 - 4 11 - 5	

TYPE	BOOT_CFG2[7]	BOOT_CFG2[6]	BOOT_CFG2[5]	BOOT_CFG2[4]	BOOT_CFG2[3]	BOOT_CFG2[2]	BOOT_CFG2[1]	BOOT_CFG2[0]
QSPI	Reserved	SPHS: Half Speed Phase Selection 0 - Select sampling at inverted clock 1 - Select sampling at inverted clock	HDSL: Half Speed Delay Selection 0 - 1-ns clock delay 1 - 2-ns clock delay	SPHS: Full Speed Phase Selection 0 - Select sampling at non-inverted clock 1 - Select sampling at inverted clock	SSL: Full Speed Delay Selection 0 - 1-ns clock delay 1 - 2-ns clock delay	Boot Frequency (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
WEIM	Moving Scheme: 00 - A/D16 01 - A+D8 10 - A+D4 11 - Reserved		OneWord Page Size: 00 - 1KB 01 - 2KB 10 - 4KB 11 - Reserved		Reserved	Boot Frequency (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
Serial-ROM	Reserved	Reserved	Reserved	Reserved	Reserved	Boot Frequency (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
SD/eSD	SD Calibration Step "00" - 1 TBD	Bus Width: 0 - 1-bit 1 - 4-bit		Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved	Boot Frequency (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD2 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved	Reserved
MMC/eMMC	Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) 111 - reserved			Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved	Boot Frequency (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD2 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved	Reserved
NAND	Toggle Mode Suspend Preamble Delay, Read Latency: 000 - 32 SPM/CLK cycles 001 - 1 SPM/CLK cycles 010 - 3 SPM/CLK cycles 011 - 3 SPM/CLK cycles 100 - 4 SPM/CLK cycles 101 - 5 SPM/CLK cycles 110 - 6 SPM/CLK cycles 111 - 7 SPM/CLK cycles			BOOT_SEARCH_COUNT: 00 - 1 01 - 2 10 - 4 11 - 8	Boot Frequency (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Boot Time "00" - 1ms "1" - 20ms (E8A NAND)	Reserved	Reserved

TYPE	BOOT_CFG4[7]	BOOT_CFG4[6]	BOOT_CFG4[5]	BOOT_CFG4[4]	BOOT_CFG4[3]	BOOT_CFG4[2]	BOOT_CFG4[1]	BOOT_CFG4[0]
0x450	Infinite-Loop (Debug USE only) 0 - Disable 1 - Enable	EEPROM Recovery Enable 0 - Disabled 1 - Enabled	CS select (SPI only): 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3		SPI Addressing: 0 - 2-bytes (16-bit) 1 - 3-bytes (24-bit)		Port Select: 000 - eSPI1 001 - eSPI2 010 - eSPI3 011 - eSPI4 100 - Reserved 101 - Reserved 110 - Reserved 111 - Reserved	
0x460	L2_HW_INVALIDATE_DISABLE	Reserved	FORCE_COLD_BOOT (Reflected in SBMR2)	BT_FUSE_SEL	DIR_BT_DIS	Reserved	SEC_CONFIG[1]	Reserved
0x460	Reserved (DDR3 config options)							
0x460	JTAG_SMODE[1:0]	WDOG_ENABLE 0 - Disabled 1 - Enabled	SJC_DISABLE	Reserved	Reserved	Reserved	Reserved	Reserved
0x460	Reserved	Reserved	Reserved	TZASC_ENABLE	JTAG_HEO	KTE	Reserved	DLL_ENABLE 0 - Disable DLL for SD/eMMC 1 - Enable DLL for SD/eMMC
0x470	DLL Override: 0 - DLL Slave Mode for SD/eMMC 1 - DLL Override Mode for SD/eMMC	Reserved	SD2 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved	Disable SDDMM Manufacture mode 0 - Enable 1 - Disable	L1 I-Cache DISABLE	BT_MMU_DISABLE	Override Pad Settings (using PAD_SETTINGS value)
0x470	Reserved for unexpected requirements	EMMC 4.4 - RESET to PRE-IDLE STATE	Override HYS bit for SD/MMC pads	USDMC_PAD_PULL_DOWN 0 - no action 1 - pull down	ENABLE_EMMC_23K_PULLUP 0 - 47K pullup 1 - 22K pullup	ADD_DS_SET_GPR1_16 0 - Set 1 - Don't set	USDMC_IOMUX_SION_BIT_ENABLE 0 - Disable 1 - Enable	USDMC_IOMUX_SRE Enable 0 - Disable 1 - Enable
0x470	USDMC_CMD_OE_PRR_EN (SD/MMC debug)	LPB_BOOT (Core / DDR - Bus) "00" - LPB Disable "01" - 1 GHz (def freq) "10" - Div by 2 "11" - Div by 4		BT_LPB_POLARITY (GPIO polarity)		POWER_MNG_CFG (LDO's DCDCs) (Reserved - NOT USED)		
0x470	Override NAND Pad Settings (using PAD_SETTINGS value)	MMC_DLL_DLY[6:0] Delay target for SD/eMMC DLL, it is applied to slave mode target delay or override mode target delay depends on DLL Override fuse bit value.						